RAW 2014

21st Reconfigurable Architectures Workshop

May 18-19, 2014 Phoenix, USA

www.ece.lsu.edu/vaidy/raw

The 21st Reconfigurable Architectures Workshop (RAW 2014) will be held in Phoenix, USA in May 2014. RAW 2014 is associated with the 28th Annual International Parallel & Distributed Processing Symposium (IPDPS 2014) and is sponsored by the IEEE Computer Society Technical Committee on Parallel Processing. The workshop is one of the major meetings for researchers to present ideas, results, and on-going research on both theoretical and practical advances in Reconfigurable Computing.

A reconfigurable computing environment is characterized by the ability of underlying hardware architectures or devices to rapidly alter (often on the fly) the functionalities of their components and the interconnection between them to suit the problem at hand. The area has a rich theoretical tradition and wide practical applicability. There are several commercially available reconfigurable platforms (FPGAs and coarse-grained devices) and many modern applications (including embedded systems and HPC) use reconfigurable subsystems. An appropriate mix of theoretical foundations and practical considerations, including algorithms architectures, applications, technologies and tools, is essential to fully exploit the possibilities offered by reconfigurable computing. The Reconfigurable Architectures Workshop aims to provide a forum for creative and productive interaction for researchers and practitioners in the area.

Topics of Interest

Authors are invited to submit manuscripts of original unpublished research in all areas of reconfigurable systems, including architectures, algorithms, applications, software and cross-cutting areas. Topics of interest include, but are not limited to:

Architectures & Algorithms

- Theoretical Interconnect and Computation Models
- Algorithmic Techniques and Mapping
- Run-Time Reconfiguration Models and Architectures
- Emerging Technologies (optical models, 3D Interconnects, devices)
- Bounds and Complexity Issues
- Analog Arrays

Reconfigurable Systems & Applications

- Reconfigurable accelerators (HPC, Bioinformatics, Multicore environments)
- Embedded systems and Domain-Specific solutions (Digital Media, Gaming, Automotive applications)
- Distributed Systems & Networks
- Wireless and Mobile Systems
- Emerging applications (Organic Computing, Biology-Inspired Solutions)
- Critical issues (Security, Energy efficiency, Fault-Tolerance)

Software & Tools

- High-Level Design Methods (Hardware/Software co-design, Compilers)
- System Support (Soft processor programming)
- Runtime Support
- Reconfiguration Techniques (reusable artifacts)
- Simulations and Prototyping (performance analysis, verification tools)

Submission Guidelines:

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript or, in special cases, may be a summary of relevant work. The manuscript should be not exceed 8 single-spaced, double-column pages using 10-point size font on 8.5X11 inch pages (IEEE conference style) including references, figures and tables. Papers are to be submitted through EasyChair. Submitted papers should not have appeared in or be under consideration for a different workshop, conference or journal. It is also expected that all accepted papers (regular or poster) will be presented at the workshop by one of the authors. IEEE CS Press will publish the IPDPS symposium and workshop abstracts as a printed volume. The complete symposium and workshop proceedings will also be published by IEEE CS Press as a CD-ROM disk.

Important Dates:

Submission deadline	December 9, 2013
Decision notification	January 20, 2014
Camera-Ready papers due	March 18, 2014

Organization:

Workshop Chairs: Jürgen Becker, Karlsruhe Institute of Technology, Germany — becker@kit.edu
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Program Chair: Marco Santambrogio, Politecnico di Milano, Italy — marco.santambrogio@polimi.it

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